WHAT IS CLAIMED IS:

1. A framework for a south bridge and a north bridge connecting, comprising:

a north bridge, including:

a memory controller, connected to a random access memory to control memory access;

a PCI response, connected to said memory controller and a PCI bus for data response process; and

a master bus arbiter, connected to said PCI response and having a plurality of request signal terminals and a plurality of grant signal terminals respectively connected to apparatuses on said PCI bus to arbiter said right of using said PCI bus for said apparatus; and

a south bridge with a high speed bus interface, including:

a direct memory access engine, with an output terminal to output a direct memory access request signal;

an up/down controller, connected to said output terminal of said direct memory access engine to receive said direct memory access request signal to control data transmission direction, said up/down controller having a plurality of output terminals;

a PCI master controller, connected to said PCI bus and one of said output terminals of said up/down controller, so as to automatically output a data access transaction to said PCI bus when said output terminal is outputting said direct memory access request signal; and

a sub-bus arbiter, connected to said PCI master controller and having a plurality of request signal terminals and a plurality of grant signals respectively connected

to said master bus arbiter of said north bridge.

2. The framework according to claim 1, wherein said south bridge further comprises a PCI response connected to said PCI bus as said PCI master controller to respond to requests sent from said apparatuses on said PCI bus.

3. The framework according to claim 2, wherein said PCI response is disabled.

4. The framework according to claim 1, wherein one of said output terminals of said up/down controller is connected to said high speed bus interface, and another is connected to said PCI master controller.

5. The framework according to claim 4, wherein said output terminal connected to said high speed bus interface is disabled.

6. The framework according to claim 1, wherein said request signal terminals and said grant signal terminals of said master bus arbiter are simultaneously connected to said request signal terminals and said grant signal terminals of said sub-bus arbiter.

7. The framework according to claim 6, wherein said master bus arbiter controls operations of said sub-bus arbiter to ensure a fluent data access of said apparatuses on said PCI bus, said south bridge and said north bridge.

8. The framework according to claim 7, wherein said sub-bus arbiter is connected to said PCI master controller to request a redirection of data transmission.

9. A framework, comprising:

a north bridge with a high speed bus interface, including:

a memory controller, connected to a random access memory to control memory access, so as to determine whether data transmission on a PCI bus is granted;

a high speed bus, connected to said north bridge for data transmission thereof; and

a south bridge with a high speed bus interface, including:

a direct memory access engine, with an output terminal to output a direct memory access request signal;

an up/down controller, connected to said output terminal of said direct memory access engine to receive said direct memory access request signal to control data transmission direction, said up/down controller having a plurality of output terminals, and one of which is connected to said high speed bus for high speed data transmission to said north bridge;

a PCI master controller, connected to said PCI bus and another output terminal of said up/down controller, so as to automatically output a data access transaction to said PCI bus when said output terminal is outputting said direct memory access request signal; and

a sub-bus arbiter, connected to said PCI master controller and having a plurality of request signal terminals and a plurality of grant signals respectively connected

to said master bus arbiter of said north bridge.

10. The framework according to claim 9, wherein said up/down controller builds up a data access to said north bridge according to said direct memory access request output from said direct memory access engine.

11. The framework according to claim 9, wherein said up/down controller builds up a data access to said PCI bus according to said direct memory access request output from said direct memory access engine.

12. The framework according to claim 9, wherein said south bridge further comprises a PCI response connected to said PCI bus as said PCI master controller to respond to requests sent from said apparatuses on said PCI bus.

13. A framework, comprising:

a north bridge, providing either one of a high speed bus interface and a PCI bus interface; and

a south bridge, having both a high speed bus interface and a PCI bus interface, to selectively provide compliance with said interface provided by said north bridge.

14. The framework according to claim 13, wherein said south bridge further comprises:

a direct memory access engine, with an output terminal to output a direct memory

access request signal;

an up/down controller, connected to said output terminal of said direct memory access engine to receive said direct memory access request signal to control data transmission direction, said up/down controller having a plurality of output terminals;

a PCI master controller, connected to said PCI bus and another output terminal of said up/down controller, so as to automatically output a data access transaction to said PCI bus when said output terminal is outputting said direct memory access request signal; and

a sub-bus arbiter, connected to said PCI master controller and having a plurality of request signal terminals and a plurality of grant signals respectively connected to said master bus arbiter of said north bridge.

15. The framework according to claim 14, wherein said south bridge further comprises a PCI response connected to said PCI bus as said PCI master controller to respond requests sent from said apparatuses on said PCI bus.

16. The framework according to claim 15, wherein said PCI response is disabled.

17. The framework according to claim 4, wherein one of said output terminals of said up/down controller is connected to said high speed bus interface, and another output terminal of said up/down controller is coupled to said PCI master controller.